120. (New) A system for storing an error checking and correcting (ECC) bit in a three-dimensional memory array of memory cells in a memory device, the system comprising:

a memory device comprising a three-dimensional memory array of memory cells; and

a data storage system coupled with the memory device and comprising an error checking and correcting (ECC) code generator, wherein the data storage system is operative to store at least one data bit and at least one error checking and correcting (ECC) bit generated by the ECC code generator based on the at least one data bit in the three-dimensional memory array in the memory device.

121. (New) The invention of Claim 120, wherein the ECC code generator comprises software in the data storage system.

122. (New) The invention of Claim 120, wherein the data storage system comprises a file system, and wherein the ECC code generator is part of the file system.

123. (New) The invention of Claim 120, wherein the ECC code generator comprises hardware in the data storage system.

124. (New) The invention of Claim 120, wherein the memory cells comprise write-once memory cells.

125. (New) The invention of Claim 120, wherein the memory cells of the three-dimensional memory array are arranged in a plurality of vertically-stacked layers.